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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/814,949

03/30/2004

Andrew Crosland

15114H-073800US

8275

26059

7590

10/05/2006

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER

SHIN, CHRISTOPHER B

ART UNIT

PAPER NUMBER

2181

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/814,949

Applicant(s)

CROSLAND ET AL.

Examiner

Christopher B. Shin

Art Unit

2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-36 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Drawings

1. The drawings were received on August 10, 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-19 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Tokieda et al. (5,511,013).

- a. The Tokieda reference teaches all of the limitations of the claimed limitations as follows:

<u>Claims 1-19</u>	<u>Tokieda et al. (5,511,013)</u>
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- A microprocessor-based system, comprising at least one peripheral device
 - Figure 3
- an address map for storing addresses allocated to the or each peripheral device
 - (17)
- When the peripheral device is disabled, the peripheral device is automatically removed from the address map
 - (171-174)
- A peripheral control register, and further comprising clock generating logic associated with each peripheral device,
 - (91-94, 101-104, 111-114, 121-124 Combination of (17) & (91-94, 101-104, 111-114, 121-124)

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- Wherein a peripheral device may be disabled by sending a logic signal from the peripheral control register to the clock generating logic associated with said peripheral device
 - Combination of (17) & (91-94, 101-104, 111-114, 121-124)
- When said logic signal is sent from the peripheral control register to the clock generating logic associated with said peripheral device, a corresponding logic signal is also sent to said address map to remove said peripheral device from the address map
 - Combination of (17) & (91-94, 101-104, 111-114, 121-124)
- Having a programmable address map,
 - (17)
- wherein, when the peripheral device is removed from the address map, a clock signal is automatically gated off from the peripheral device
 - Combination of (17) & (91-94, 101-104, 111-114, 121-124)
- Clock generating logic associated with each peripheral device
 - (91-94, 101-104, 111-114, 121-124)
- when the peripheral device is removed from the address map, a logic signal is sent to said clock generating logic to gate off the clock signal from the peripheral device, and thereby disable the peripheral device
 - Combination of (17) & (91-94, 101-104, 111-114, 121-124)
- Clock generator for supplying a clock signal to each peripheral device, through the associated clock generation logic
 - (10) supply to (41-44) through (91-94, 101-104, 111-114, 121-124)
- wherein the system is implemented in an integrated circuit and wherein the peripheral devices comprises an interface for an external device
 - column 1, lines 6-30
- wherein the system is implemented in a programmable IC and the microprocessor is provided as an embedded device, at least one of the peripheral device is implemented in programmable logic
 - obvious features of column 1, lines 6-30

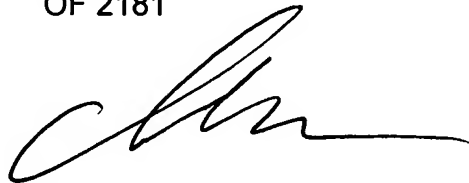
b. Since the Tokieda reference teaches substantially identical or functionally equivalent limitations of the claimed invention, one skilled in the art can easily come up with the claimed invention from the teachings of the Tokieda reference.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher B. Shin whose telephone number is 571-272-4159. The examiner can normally be reached on 6:30-5:00 M,Tu,Th,F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CHRISTOPHER SHIN
PRIMARY EXAMINER
OF 2181



September 24, 2006
Cbs